

IN THE SPECIFICATION:

Please amend paragraph number [0006] as follows:

[0006] Moreover, some semiconductor dice have bond pads that are positioned in locations that will not adequately and stably support these dice when conductive structures are secured thereto and the dice are disposed face down (i.e., in a flip-chip orientation) over a higher level substrate. Examples of such dice include leads-over-chip (LOC)-configured semiconductor dice and semiconductor dice with one or two rows of bond pads along the central axes of the dice with bond pads positioned adjacent only a single peripheral edge thereof. Thus, when conductive structures are secured to the bond pads of such a semiconductor die and the semiconductor die is then positioned face down relative to a higher level substrate, the die is prone to being tipped or tilted from an intended orientation that is substantially parallel to a plane of the ~~contact-pad-bearing~~ pad-bearing surface of the higher level substrate. As a consequence, such dice are thought to be unsuitable for flip-chip applications without rerouting of the bond pads to a more stable arrangement. In addition, one or two rows of bond pads bearing solder bumps may not exhibit sufficient surface tension during reflow of the solder to support the die, resulting in collapse or flattening of the masses of molten solder and shorts of adjacent connections. Inadequate support strength may also be a problem with other materials.

Please amend paragraph number [0059] as follows:

[0059] If the conductive material of the conductive structures, such as solder bumps 30, will sag when reflowed, stabilizers 50 may protrude from active surface 14 a greater distance 54 than the distance 60 that conductive structures, such as solder bumps 30, protrude from active surface 14. Such sagging of the conductive material during reflow facilitates the formation of electrical connections between bond pads 12 and contact pads 40 even when ~~spacers~~ stabilizers 50 are taller than the conductive structures. Thus, the use of taller ~~spacers~~ stabilizers 50 may facilitate the formation of taller, thinner conductive structures.

Please amend paragraph number [0081] as follows:

[0081] Referring now to FIGs. 20 and 21, data from the STL files resident in computer 82 is manipulated to build an object, such as stabilizers ~~50~~ 50, illustrated in FIGs. 8-19 ~~and 22 or 22~~, or base supports 122, one layer at a time. Accordingly, the data mathematically representing one or more of the objects to be fabricated are divided into subsets, each subset representing a slice or layer of the object. The division of data is effected by mathematically sectioning the 3-D CAD model into at least one layer, a single layer or a "stack" of such layers representing the object. Each slice may be from about 0.0001 to about 0.0300 inch thick. As mentioned previously, a thinner slice promotes higher resolution by enabling better reproduction of fine, vertical surface features of the object or objects to be fabricated.

Please amend paragraph number [0088] as follows:

[0088] In practicing the present invention, a commercially available stereolithography apparatus operating generally in the manner as that described above with respect to apparatus 80 of FIG. 20 is preferably employed, but with further additions and modifications as hereinafter described for practicing the method of the present invention. For example and not by way of limitation, the SLA-250/50HR, SLA-5000 and SLA-7000 stereolithography systems, each offered by 3D Systems, Inc. of Valencia, California, are suitable for modification. Photopolymers believed to be suitable for use in practicing the present invention include Cibatool SL 5170 and SL 5210 resins for the SLA-250/50HR system, Cibatool SL 5530 resin for the SLA-5000 and 7000 systems, and Cibatool SL 7510 resin for the SLA-7000 system. All of these photopolymers are available from Ciba Specialty Chemicals ~~Corporation~~ Inc.

Please amend paragraph number [0095] as follows:

[0095] Continuing with reference to FIGs. 20 and 21, the semiconductor device or devices 10 on platform 90 may then be submerged partially below the surface level 88 of liquid material 86 to a depth greater than the thickness of a first layer of material 86 to be at least partially consolidated (e.g., cured to at least a semisolid state) to form the lowest layer 130 of

each stabilizer 50 at the appropriate location or locations on each semiconductor device 10, then raised to a depth equal to the layer thickness, surface level 88 of material 86 being allowed to become calm. Photopolymers that are useful as material 86 exhibit a desirable dielectric constant, low shrinkage upon cure, are of sufficient (i.e., semiconductor grade) purity, exhibit good adherence to other semiconductor device materials, and have a sufficiently similar coefficient of thermal expansion (CTE) to the material of the conductive structures (e.g., solder or other metal or metal alloy). As used herein, the term "solder ball" may also be interpreted to encompass conductive or conductor filled epoxy. Preferably, the CTE of material 86 is sufficiently similar to that of the conductive structures to prevent undue stressing of the conductive structures or of semiconductor device 10 during thermal cycling thereof in testing and subsequent normal operation. One area of particular concern in determining resin suitability is the substantial absence of mobile ions and, specifically, of fluoride ions. Exemplary photopolymers exhibiting these properties are believed to include, but are not limited to, the above-referenced resins from Ciba Specialty ~~Chemical Company~~. Chemicals Inc.

Please amend paragraph number [00105] as follows:

[00105] While a variety of methods may be used to fabricate stabilizers 50, the use of a stereolithographic process as exemplified above is a preferred method because a large number of stabilizers 50 may be fabricated in a short time, the stabilizer height and position are ~~computer-controlled~~ computer-controlled to be extremely precise, wastage of unconsolidated material 86 is minimal, solder coverage of passivation materials is reliably avoided through precise spacer height control, and the stereolithography method requires less handling of semiconductor devices 10 or other substrates than the other viable methods indicated above.